## REMARKS

The rejections presented in the Office action dated October 6, 2003 have been considered. Claims 1-3, 5-20 and 22 remain pending in the application. Reconsideration and allowance of the application as amended is respectfully requested.

Claims 1-7, 11-12, 14-15, and 17-22 stand rejected under 35 U.S.C. §102(b) as being unpatentable over *La Fetra* (U.S. Patent No. 5,509,119). The Applicants respectfully traverse the Examiner's rejection.

With respect to independent Claim 1, the Examiner asserts that *La Fetra* describes performing a first comparison of the memory access address to the stored tag address. The Examiner cites from column 2, line 5 *et seq.* of *La Fetra* stating that *La Fetra*'s second comparator 401 is provided which receives the Cache-Tag/Cache-ECC pair from the cache RAM 205, and that another input of the second comparator 401 receives the CPU address Tag 403 and a derived CPU-Tag ECC generated by an ECC generator 405. This indicates that the first comparator 401 of *La Fetra* compares ECC-protected address tags. As stated in Applicants' background of the invention:

> Prior art systems have also utilized multiple error correction codes, requiring additional memory capacity to house all of the ECC information. Further, these prior art systems perform a comparison of all bits, including ECC bits, which adversely affects performance. (p.3, lines 4-7)
>
> ...
>
> It is important to note that in accordance with a preferred embodiment of the present invention, only the address bits are compared at the fast hit address compare 504. No ECC bits are compared. This allows fewer bits to be compared by the compare logic, thereby increasing the compare speed in the fast hit path. By using a smaller compare, a faster cycle time can be used, thus increasing performance. (p.20, lines 14-19).

As can be seen, one asserted advantage of the present invention is that ECC bits do not need to be compared in connection with the fast hit comparison. *La Fetra* clearly indicates, as the Examiner confirmed, that a Cache-Tag/Cache-ECC pair is compared to the CPU address Tag 403 and a derived CPU-Tag ECC generated by an ECC generator 405. This differs from Claim 1 which performs a fast hit comparison of the memory access address to the stored tag address, without regard to any error correction code associated with the stored tag address.

In order to facilitate prosecution of the application, Claim 1 has been amended to more particularly set forth that no such comparison of ECC portions is involved with respect to Claim 1. *La Fetra* fails to teach a comparison of a memory access address and a stored tag address without regard to any ECC that may be associated with the stored tag address. For at least this reason, *La Fetra* fails to anticipate Claim 1, and Claim 1 is in condition for allowance.

Error monitoring of Claim 1 is performed contemporaneously with the first comparison, thereby allowing the first comparison to immediately begin its comparison. As an example, the SBE error detection 510 of Applicants' FIG. 5 illustrates that the fast hit address compare 504 is performed in parallel with error detection 510. This parallel error detection allows for a comparison of the memory access address to the stored tag address without the need to compare ECCs. This is not the case with *La Fetra* where ECC generation (*e.g.*,, ECC GEN 405) is required prior to performing any comparison, which is required because *La Fetra* compares ECC-protected information.

The Examiner further indicates that *La Fetra* discloses monitoring for errors in the stored tag address, and cites the "Tag check and correct circuit 215" of *La Fetra* as teaching such function. As shown in FIG. 4 of *La Fetra*, such circuit 215 is used only in the path of the "True Hit" 225, and is therefore not used in the "Fast Hit" 407 path. Instead, the ECC generator 405 generates a new ECC which is associated with the CPU-Tag, and then compared to the Cache-Tag/Cache-ECC pair from the cache RAM 205. Therefore, it is noted for development of the discussion below that the *La Fetra* describes, as confirmed by the Examiner, that any error monitoring that is performed contemporaneously with *La Fetra*'s fast hit path is used only in the path leading to the True Hit 225.

Claim 1 includes the use of results from the first comparison or the second comparison to determine whether requested data is stored in the cache memory, based on whether a tag address error is detected in the stored tag address. Thus, the result of the error monitoring is used to determine whether the fast hit or slow hit path will be used, and is performed in parallel with the comparison of the memory access address (*e.g.*, set address 502) and corresponding tag ram address. This provides an output at the fast hit

address compare 504 more quickly. A fast hit can then be blocked (*e.g.*, block 516) if the fast hit should not be used due to the detection of an error.

*La Fetra*, on the other hand, describes a system where an input of the fast hit comparator 401 includes a CPU address Tag and a derived CPU-Tag ECC generated by an ECC generator 405 (*e.g.*, col. 5, lines 4-6). As shown in FIG. 4 of *La Fetra* and its corresponding description (*e.g.*, col. 5, lines 7-9), the ECC generator 405 computes an ECC for the CPU-Tag in a serial manner. Thus, the second comparator 401 of *La Fetra* cannot provide an output until the ECC generator 405 has completed the generation of the ECC. This is clearly a serial operation, first requiring the generation of an ECC followed by a comparison of tag/ECC pairs.

Therefore, *La Fetra*'s generation of an ECC (*e.g.*, ECC GEN 405) cannot read on the error monitoring of Claim 1, as it is not performed contemporaneously with the comparison (*e.g.*, 401) of *La Fetra*. Further, the Examiner's assertion that *La Fetra* describes error monitoring by way of its "Tag check and correct circuit 215" cannot read on the error monitoring of Claim 1, as it is not used to determine which of the first or second comparisons is used to determine whether the data is stored in the cache. More particularly, Claim 1 indicates that using the first or second comparison is based on whether or not a tag address error is detected in the stored tag address, but the "Tag check and correct circuit 215" of *La Fetra* does not make such determination - rather the ECC generator 405 based on the generation of ECC and the comparison of ECCs are used.

For at least this additional reason, *La Fetra* fails to teach all of the features of Claim 1 as is required to anticipate Claim 1, and Claim 1 is in condition for allowance.

Dependent Claims 2-3 and 5-7, which are dependent from independent Claim 1, were also rejected under 35 U.S.C. §102(b) as being unpatentable over *La Fetra*. While the Applicants do not acquiesce with the particular rejections to these dependent claims, these rejections are moot in view of the amendments and remarks made in connection with independent Claim 1. Dependent Claims 2-3 and 5-7 are therefore also in condition for allowance, as these dependent claims include all of the limitations of the base claim and any intervening claims, and recite additional features which further distinguish these claims from *La Fetra*.

As an example, dependent Claim 2 is considered. The Examiner alleges that *La Fetra* discloses monitoring for errors through storage of a single error correction code with the data stored in the tag memory, particularly at *La Fetra*'s FIG. 2, element 205. Claim 2 has been amended to more particularly indicate that one embodiment of the invention involves identifying an error using a single ECC associated with the stored tag address. The Applicants respectfully submit that Claim 2 is not anticipated by *La Fetra*, and is in condition for allowance.

Furthermore, it is noted that a fundamental principle of *La Fetra* is to split the ECC into multiple parts. (*e.g.*, col. 4, lines 46-59), where Claim 2 involves the use of a single ECC. *La Fetra* does not teach the use of a single ECC in such a system. FIG. 2 of *La Fetra* shows a single ECC used in a prior art system that does not involve the use a fast hit processing path. *La Fetra* teaches that to use such a fast hit processing path 407, the ECC must be split into two ECCs. Examples of this in *La Fetra* include:

> *The present invention divides the ECC segment 107 into two segments* where one ECC segment protects the Cache-Tag 103 and one segment protects the unpredictable information in segment 105. FIG. 3 illustrates a cache entry 301 according to the present invention.
>
> Segments 103 and 105 are the same as previously described. *However, the ECC segment 107 in FIG. 1 has been split into two segments 307 and 309*. ECC segment 307 protects the Cache-Tag 103 and ECC segment 309 protects segment 105.
>
> *Since the ECC has been split*, the ECC segment 307 associated with the Cache-Tag 103 can be predicted (for a hit to occur) given a CPU-Tag This is true as the method of generating an ECC is known, so given a specific Tag, the associated ECC can be readily determined. Therefore both the Cache-Tag 103 and the associated Cache-ECC 307 can be predicted given a specific CPU-Tag, again assuming a cache hit is to occur. (col. 4, lines 46-64). (*emphasis added*)

Thus, there is no teaching of using a single ECC in connection with a system that implements a fast and slow hit path. To anticipate a claim, the identical invention must be shown in as complete detail as is contained in the claim, *and the elements must be arranged as required by the claim.* M.P.E.P. § 2131. The Applicants contend that *La Fetra* fails to describe any system using a fast hit path 407 and a true hit path 225 that does not involve the splitting of an ECC into multiple parts. Because the identical invention

must be shown in as complete detail as is contained in the claim, and *the elements must be arranged as required by the claim*, it is respectfully submitted that *La Fetra* fails to anticipate Claim 2, and for at least this additional reason Claim 2 is allowable over *La Fetra*. Dependent Claim 3 is dependent from dependent Claim 2, includes all of the limitations of Claim 2, and recites additional features which further distinguish it from *La Fetra*. Therefore, dependent Claim 3 is also in condition for allowance.

Independent Claim 11 has also been rejected as being anticipated by *La Fetra*. The Applicants respectfully traverse the rejection. First, the Examiner argues that *La Fetra* teaches "an error detector coupled to the tag memory to receive the tag address and to determine whether there are any errors in the tag address." The Applicants contend that this correlation is incorrect. The Examiner identified the ECC generator 405 of *La Fetra* as teaching the error detector of Claim 11, however the ECC generator 405 of *La Fetra* does not receive the tag address, and consequently cannot determine whether there are any errors in the tag address. Rather, the ECC generator 405 receives the CPU address, and generates an ECC in order to compare the Cache-Tag/Cache-ECC pair to the CPU-Tag and generated ECC. Therefore, the ECC generator 405 of *La Fetra* fails to teach an error detector coupled to the tag memory to receive the tag address and to determine whether there are any errors in the tag address. For at least this reason, *La Fetra* fails to anticipate independent Claim 11.

Further, the Examiner argues that *La Fetra* teaches a gated output module coupled to the first address compare module and the error detector. The Applicants respectfully contend that this correlation is incorrect. The Examiner identifies the second comparator 401 of *La Fetra* as the gated output module, which is coupled to the first address compare module and the error detector. The Examiner thus argues that the second comparator 401 of *La Fetra* is both the first address compare module and the gated output module of Claim 11. No such gating function coupled to *La Fetra*'s second comparator 401 is described in *La Fetra*. Because the identical invention must be shown in as complete detail as is contained in the claim, and *the elements must be arranged as required by the claim*, it is respectfully submitted that *La Fetra* fails to anticipate Claim 11 for at least this additional reason.

The rejection to independent Claim 18 is traversed for similar reasons, as *La Fetra* fails to teach at least an error detector coupled to the tag memory to receive the tag address and to determine whether there are any errors in the tag address, and an error detector coupled to the tag memory to receive the tag address and to determine whether there are any errors in the tag address. Since *La Fetra* fails to teach at least these elements, *La Fetra* cannot anticipate independent Claim 18, and Claim 18 is allowable over *La Fetra*.

The Applicants submit that the Examiner's rejection of independent Claims 11 and 18 include errors of finding of fact, which has led to a rejection that is grounded in an error of law. The Applicants respectfully submit that the resulting error of law compels reversal of this rejection, as anticipation of Claims 11 and 18 has not been established.

Dependent Claims 12, 14, 15 and 17 which are dependent from independent Claim 11, and dependent Claims 19 and 20 which are dependent from independent Claim 18, were also rejected under 35 U.S.C. §102(b) as being unpatentable over *La Fetra*. While the Applicants do not acquiesce with the particular rejections to these dependent claims, these rejections are moot in view of the amendments and remarks made in connection with independent Claims 11 and 18. Dependent Claims 12, 14, 15, 17, 19 and 20 are therefore also in condition for allowance, as these dependent claims include all of the limitations of their respective base claim and any intervening claims, and recite additional features which further distinguish these claims from *La Fetra*.

Independent Claim 21 also stands rejected as being anticipated by *La Fetra*. The Applicants respectfully traverse the Examiner's rejection, as *La Fetra* fails to teach all the limitations set forth in Claim 21. Claim 21 has been canceled without prejudice or disclaimer, and Claim 22 has been rewritten in independent form. With respect to the claim recitation "means for coordinating timing between the first hit detection path means and the second hit detection path means," the Examiner argues that *La Fetra* teaches this for the following reason (citing from *La Fetra*):

> Since, most of the time the cache tag does not need to be corrected and generally there is a cache hit, by using the fast hit signal, the cache memory system can supply data to the CPU in less time than the prior art designs allow. If the fast hit is not asserted, then either there is a cache miss or the

> Cache-Tag has an error and the cache memory system waits for the true hit/miss signal as before.

It is respectfully submitted that this language does not identify the function, nor the structure of the Claim 22 element "means for coordinating timing between the first hit detection path means and the second hit detection path means." The function involves the coordination of timing between the first and second hit detection paths. The portion of *La Fetra* recited by the Examiner discusses "time" in the sense of speed or throughput. It does not teach or otherwise mention "timing" in the sense used in Claim 22. Further, the Examiner has not identified any structure in *La Fetra* that corresponds to the means to perform such function, as required by M.P.E.P. § 2106 and Federal Circuit mandate. For at least this reason, the Examiner has not established that Claim 22 is anticipated by *La Fetra*, and it is respectfully submitted that Claim 22 is in condition for allowance.

Claims 8-10, 13 and 16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *La Fetra*. The Applicants respectfully traverse the Examiner's rejection.

The Examiner first indicates that Claims 8-10, 13 and 16 are unpatentable over *La Fetra* as applied to Claims 1 and 11 above. The Applicants respectfully traverse the rejection using rationale applied to Claims 1 and 11 for reasons set forth above.

More particularly, with respect to Claim 8, the Examiner argues that *La Fetra* teaches/suggests disregarding the first comparison by blocking passage of the results of the first comparison through an output gate. With respect to Claim 9, the Examiner argues that *La Fetra* teaches/suggests that blocking passage of the results is performed by providing an error signal to the output gate when a tag address error is detected, and disabling the output of the output gate upon receipt of the error signal. The Applicants respectfully disagree.

In some embodiments of the invention, such as those set forth in Claims 8 and 9, passage of results from the first comparison are disregarded using an output gate. In these embodiments, this is a result of the contemporaneous monitoring of errors in the stored tag address, and the comparison of the memory access address and stored tag address. The result of the comparison is coupled to a gate that is controlled by the result of

the error detection. As previously noted, *La Fetra* does not perform this contemporaneous function, as it performs an ECC generation of the CPU address *before* providing the generated ECC to the comparison 401, and therefore no such gating is required in *La Fetra*, nor is it taught or suggested. The comparison 401 in *La Fetra* provides the final output, which is possible due to the serial nature of the ECC generation 405 with the comparison 401. Therefore no passage of the result of the comparison 401 is gated by anything - the output of the comparison 401 is the result. Further, Claim 9 indicates that an error signal is provided to the output gate *when a tag error is detected.* This does not occur in *La Fetra*. *La Fetra* provides a generated ECC to a comparator, and does not provide any error signal to an output gate based on detection of a tag error.

The Examiner argues that although *La Fetra* does not specifically disclose blocking passage of the results of the first comparison through an output gate by providing an error signal to the output gate when a tag address is detected and disabling an output of the output gate upon receipt of the error signal, "blocking an error signal is notoriously well known in the art." However, there is no such error signal described in *La Fetra* in which to block, and the Examiner cannot limit the inquiry to simply "blocking an error signal." For Claim 8, the inquiry must be "blocking passage of the results of the first comparison through an output gate," and for Claim 9 the inquiry must be "providing an error signal to the output gate when a tag address error is detected, and disabling an output of the output gate upon receipt of the error signal."

In order to establish *prima facie* obviousness, the Examiner has the burden of establishing that three basic criteria are met. First, there must be some suggestion or motivation to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on the Applicants' disclosure. All three of these criteria must be met in order to support a finding of *prima facie* obviousness of a claimed invention (see, e.g., MPEP § 2142).

The Applicants respectfully submit that the Examiner has not established *prima facie* obviousness for Claims 8 and 9. First, as previously indicated, Claims 8 and 9 are dependent from independent Claim 1, and *La Fetra* fails to teach, or suggest, all of the limitations of Claim 1. The Examiner has also indicated that one of ordinary skill in the art would have been motivated to block a signal on error because of the following:

> If the fast hit is not asserted, then either there is a cache miss or the Cache-Tag has an error and the cache memory system waits for the true hit/miss signal as before.

It is respectfully submitted that this purported motivation to modify *La Fetra* to arrive at the claimed invention of Claims 8 and 9 falls well short of the Federal Circuit mandate for modifying such a reference. This statement fails to provide the requisite motivation to modify *La Fetra* to arrive at a method where "blocking passage of the results of the first comparison through an output gate," and "providing an error signal to the output gate when a tag address error is detected, and disabling an output of the output gate upon receipt of the error signal." It is respectfully submitted that the Examiner has, through impermissible hindsight, used the Applicants' disclosure in an attempt to establish motivation to modify the *La Fetra* reference to arrive at Claims 8 and 9. For at least this additional reason, it is respectfully submitted that *prima facie* obviousness had not been established.

There is also no indication that there would be a reasonable expectation of success by including an output gate after *La Fetra*'s comparator 401 using the ECC generator 405 output as proposed by the Examiner. In *La Fetra*, the comparison is a comparison of 1) the CPU address tag 403 and an ECC generated by the ECC GEN 405, and 2) the Cache-Tag/Cache-ECC pair. By using the ECC generator 405 to provide an "error signal" to an output gate following the comparator 401, the desired result of *La Fetra* would not occur. In such a case, the comparator 401 could not compare what *La Fetra* indicates it must compare, which is both the addresses and the ECCs. Further, the output of the ECC generator 405 of *La Fetra* is not an error signal, but rather is a generated ECC, and therefore it is unclear how a generated ECC would control an output gate following the comparator 401. For this additional reason, it is submitted that *prima*

*facie* obviousness has not been established, and Claims 8 and 9 are therefore not rendered obvious by *La Fetra*.

Dependent Claim 10 is dependent from Claims 8 and 9, and also stand rejected under 35 U.S.C. §103(a) as being unpatentable over *La Fetra*. While Applicants do not acquiesce with any particular rejections to Claim 10, this rejection is moot in view of the remarks made in connection with Claims 8 and 9, as Claim 10 includes all of the limitations of Claims 8 and 9, and recites additional features which further distinguish it from the cited references. "If an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious." M.P.E.P. §2143.03; *citing In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Therefore, dependent Claim 10 is also allowable over *La Fetra*.

With respect to Claim 13, the Examiner admits that *La Fetra* does not specifically disclose latching as a means for coordinating timing between the fast hit detection circuit and the slow hit detection circuit. It is first noted that Claim 13 includes the limitations of Claim 11, and as previously indicated *La Fetra* fails to teach or suggest all the limitations of Claim 11. Further, there is no reasonable expectation of success in *La Fetra* to implement latching means as recited in the Applicants' Specification to coordinate timing, as the *La Fetra* system operates differently than that set forth in Claim 13. It is also respectfully submitted that the Examiner's motivation to modify *La Fetra* to implement latching means is made in hindsight, with the benefit of the Applicants' disclosure. The Examiner has not established why or where in the *La Fetra* system one of ordinary skill in the art would implement such latching means. For at least these reasons, it is respectfully submitted that *prima facie* obviousness has not been established for Claim 13, and Claim 13 is in condition for allowance.

With respect to Claim 16, the Examiner admits that *La Fetra* does not specifically disclose the entirety of Claim 16, including:

> a first latch coupled to the first address compare module to latch comparison results;
>
> a second latch coupled to the error detector to latch a resulting error indicator signal; and
>
> wherein the comparison results and the error indicator signal are not passed to the gated output until both the comparison results and the error

indicator signal are available at the first and second latches, and until simultaneously clocked to concurrently provide the comparison results and the error indicator signal to the gated output.

The Examiner argues, however, that a person of ordinary skill in the art would have been motivated to do so. It is respectfully submitted that such an assertion is made through impermissible hindsight, using the Applicants' disclosure as a blueprint for piecing together the *La Fetra* reference and what is purportedly known in the art to defeat patentability. The Examiner has not established why one of ordinary skill in the art would use such latches in connection with *La Fetra* at all, much less to use such latches to arrive at the invention set forth in Claim 16. The fact that latching is a known general concept does not relieve the Examiner from establishing a motivation to modify the *La Fetra* reference to arrive at the claimed invention. It is respectfully submitted that this motivation has not been established, and therefore *prima facie* obviousness has not been established for at least this reason. Claim 16 is therefore not rendered obvious by *La Fetra*, and is in condition for allowance.

## CONCLUSION

The Applicants respectfully submit that the pending claims are patentable over the cited prior art of record, and that the application is in condition for allowance. If the Examiner believes it necessary, the undersigned attorney of record may be contacted at (651) 686-6633 (x110) to discuss any issues related to this case.

Respectfully submitted,

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